CLAIMS

1. A circuit for reducing standby leakage in a memory unit, comprising:

a capacitive divider coupled to the memory unit so as to generate a voltage across the memory unit, the voltage being adequate to retain memory values during one of a sleep state and a standby state.

2. The circuit according to claim 1, wherein said capacitive divider is coupled to the memory unit on-chip.

3. The circuit according to claim 1, wherein the voltage is a division of a normal operating voltage.

4. The circuit according to claim 3, wherein the voltage is substantially Vdd/2.

5. The circuit according to claim 3, wherein the voltage is substantially Vdd/3.

6. The circuit according to claim 1, wherein said

capacitive divider is configured for varying an oscillator frequency in accordance with the generated voltage so as to minimize switching losses.

7. The circuit according to claim 1, wherein the memory unit is coupled between Vss and Vddinternal terminals.

8. The circuit according to claim 1, wherein the memory unit is coupled between Vdd and Vddinternal terminals.

9. The circuit according to claim 1, wherein the memory unit is coupled between a first Vddinternal and a second Vddinternal terminal at a different potential.

10. An integrated circuit for reducing standby leakage in a memory unit, comprising:

a substrate having a capacitive divider coupled to the memory unit so as to generate a voltage across the memory unit, the voltage being adequate to retain memory values during one of a sleep state and a standby state.

11. An inductive circuit for reducing standby leakage in a memory unit, comprising:

an inductive divider coupled to the memory unit so as to generate a voltage across the memory unit, the voltage being adequate to retain memory values during one of a sleep state and a standby state.

12. The inductive circuit according to claim 11, wherein said inductive divider is coupled to the memory unit on-chip.

13. The inductive circuit according to claim 11, wherein the voltage is a division of a normal operating voltage.

14. The inductive circuit according to claim 13, wherein the voltage is substantially Vdd/2.

15. The inductive circuit according to claim 13, wherein the voltage is substantially Vdd/3.

16. The inductive circuit according to claim 11, wherein said inductive divider is configured for varying an oscillator frequency in accordance with the generated voltage so as to minimize switching losses.

17. The inductive circuit according to claim 11, wherein the memory unit is coupled between Vss and Vddinternal terminals.

18. The inductive circuit according to claim 11, wherein the memory unit is coupled between Vdd and Vddinternal terminals.

19. The inductive circuit according to claim 11, wherein the memory unit is coupled between a first Vddinternal and a second Vddinternal terminal at a different potential.

20. An integrated inductive circuit for reducing standby leakage in a memory unit, comprising:

a substrate having an inductive divider coupled to the memory unit so as to generate a voltage across the memory unit, the voltage being adequate to retain memory values during one of a sleep state and a standby state.